Original Article

Vlsi Implementation Of Ternary Adder And Multiplier Using Tanner Tool

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Abstract

In CMOS logic, only binary logic is taken into consideration for implementation. Binary connection increases in size on the VLSI chip with circuit complexity, degrading performance. The proposed answer to this problem is in MVL (Multi valued logic).The optimal radix for many MVL systems is ternary logic, which is often referred to as three-valued logic.The layout is made with the use of VLSI CMOS technology, and the proposed ADDER AND MULTIPLIER is developed and simulated using the Microwind EDA tool.

Keyword: Ternary Adder, Ternary multiplier, VLSI

I. INTRODUCTION

Recent advances in multimedia and mobile computing applications necessitate VLSI digital signal processing systems with low power and high performance[1].When creating digital systems, three valued logic, sometimes referred to as ternary logic, provides numerous significant benefits over binary logic.For instance, more data can be transmitted along a predetermined number of lines or stored for a predetermined amount of time in a register, connection complexity, chip area can be reduced, aerror-detection and error-correction codes can be employed more effectively. Additionally, faster performance can be achieved for various serial-parallel and serial arithmetic processes. Because most of these benefits are directly related to the VLSI digital system implementation systems, a variety of various realizations of fundamental quaternary gates have been proposed in the literature. These have proven beneficial for a variety of tasks, including as refers to the experience and the construction of "ternary computers." [2].

Three-valued flipping and transmission is referred to as ternary. Three-valued logic, often known as ternary logic, has numerous significant benefits over binary logic when it comes to developing digital systems.For instance, more data may be conveyed along a set of lines or retained for a fixed amount of time, connectivity complexity may be reduced, chip space may be reduced, and error detection and correction codes may be employed more effectively. Additionally, faster performance can be achieved for various serial-parallel and serial arithmetic processes. Many of these benefits have a direct impact on the implementation of computer data, resulting in the creation of fundamental ternary gate realisations. These have been shown to be perfect for developing "ternary processors" in addition to a number of other applications [3]. Since ternary logic achieves high data transmission through connective lines, it generally requires fewer components and interconnections. As a result, it requires less storage than binary to provide the same functionalities. As a result, it can swiftly and effectively analyze data [4].

In recent years, system designers have become increasingly interested in studying fast multiplier design. The use of parallel multiplication algorithms has increased in popularity as a technique to speed up computations involving a lot of multiplications. The use of partial product grid reduction or column compression has significantly reduced the completion time for parallel multiplication.Following linear array multiplication methods have been proposed, each of which requires just u cycles of time to multiply two TI-bit integers and makes use of practically typical connection layouts of the multipliers array cellular constituents [5].

In order to build MVLsystems, complementary metal oxide semiconductors (CMOS) have dominated the semiconductor industries for decades.Two-level binary logic's performance is constrained by the link, which takes up a lot of room on a VLSI device. The ternary logic, often known as radix 3 of MVL, consists of three levels: -1, 0 and 1 for imbalanced ternary logic and 0 and one for balancing ternary logic.The binary system needs more digits than the ternary system does. As a result, more operations—like arithmetic and logic—can be completed more quickly and with fewer computational steps [6].In this study, a ternary multiplier and ternary adder VLSI designs have been developed from an arithmetic perspective. The proposed ternary multiplier and ternary adder achieved higher operating frequencies even with higher filter order thanks to their pipelined construction.

II. LITERATURE SURVEY

GTGs were proposed by Mozammel H. A. Khan et colleagues. [7] But no synthesis algorithm could directly synthesis all of these gates. In this work, we demonstrate how to build binary half- and full-adder devices using a cascade of GTGs. The ternary full-adder circuit requires four 4*4 gates, eight 3*3 gates, two 2*2 entrance, and a total of 16 gates. Our ternary complete adder circuit, however, only requires 10 2*2 gates. Since controlling the interactions of more than two substances is essentially impossible, every m*m (m > 2) gates in quantum physics is extraordinarily difficult to build. Therefore, 1*11 and 2*2 gates should be used to realize these gates. We have a superior answer than the one provided by as a result. Results from earlier versions cannot be compared since this is the first time the tripartite half-adder circuit has been created.Jihad Without the use of ternary decoders, fundamental logic gates, or ternary codecs, Mohamed Aljaamet et al. [8] introduced unique designs of 32 nm Mitigate this issue Nested loops Half Adder and Ternary Multiply employing recommended Unary Operators in combination with transmission gates. The design technique combines many strategies, such as transistor layout, two power supplies (Vdd, Vdd/2), and transistors count reduction, to produce the desired result.When compared to existing circuits, the proposed circuits perform better and use less energy under various simulation situations, such as noise effect studies and PVT (process, voltage, and temperature) changes.The findings showed that the suggested circuits were more noise-tolerant and robust to process changes than earlier models.

DhandeA. P. et al. [9] A 2-bit ALU slice's whole architecture, design, and implementation are discussed. The approach, which is based on an improved ternary logic gate, is also described. It offers significant benefits like lowered static power usage, faster operation, and simplified circuitry. By altering the decoder, selection logic, and other components, the ALU can be made to perform more tasks. It can therefore be utilized as a processing component in ternary microprocessors.

B. G. Hoskins et al.[10] VLSI parallel processor arrays have been designed for a chip. Multiplexing overcomes the 1/0 barrier, but parallel is still preserved since each PE has a two processing blocks and weights storage area. While allowing for flexibility in building a variety of network topologies, the changeable threshold, the temary input layer relaxes weight accuracy. Through the use of software simulations executed on a precision floating - point processor, the architect's trainability and effectiveness in a classification job were assessed. PES, bits per weight, and the number of discernible output levels may all be increased in the design; these features are all solely constrained by chip area.

El-Slehda A. A. et al. [11] A balanced ternary adder based on melmistors was introduced in order to achieve less area and more speed. Several examples and PSPICE circuit simulations were used to show and evaluate the memristor-based ternary adder architecture. This ternary adder can also provide a carry-free binary adding that is dependent of bit count. The concept may potentially be utilised to develop even faster systems, such multipliers.AsmaTaheriMonfared et al. [12] a new circuit for implementing ternary half-adders was presented.The development of a revolutionary parallel adder/subtracted and a quantum reversible ternary full-adder. Since we only employed a few ternary quantum gates, those adder circuits have such a reduced quantum cost.Additionally, the circuits we recommend have fewer levels and steady inputs. They perform better than earlier designs in the literature as a result. The suggested quantum irreversible ternary adder circuits can be utilized in the construction of arithmetic processor, computational circuits, and other high-end nanotechnology applications and hardware. All of the designs employed are nanometric in scale.

Martin Kumm and others, [13] It was possible to solve the pipelined multiple continuous multiplication issue using the ternary adder realizations seen in contemporary FPGAs. This method has several uses since it generalizes both single locus multiplication and multiple continuous multiplications without pipelining (with or without pipelining).In compared to a state-of-the-art technique that employs two-input adders, the number of pipelined activities (pipelined adders/subtractions and registers) may be decreased by 10% to 44% depending on the benchmark instance. Slice reduction of 5.8% up 50% and ALM reduction of up to 42% for the matching Xilinx Virtex 6 & Altera Stratix IV FPGAs were possible. The designs achieve clock rates of more than 370 MHz on Virtex 6 & 450 MHz and Stratix IV FPGAs while being lower than two-input adder realizations and having fewer pipeline stages.

Summary:

- Low-power embedded systems at the nanoscale and Internet of Things devices can use several battery-saving techniques.
- Building ternary logic functions with ternary PLAs is another way to increase packing density and implement more complex functions.

III. PROPOSED METHOD

Inverters, NOR gates, and NAND gates are thought of as the basic components of digital systems. By reducing power usage and propagation delay time, the number of transistors is primarily sought to be decreased. The suggested designs employ MOSFETs with lower threshold voltages and smaller single supply voltages States 0, 1, and 2 with possibilities (0 v), (0.5 v), and (+Vcc) (+1 v), respectively, indicate the first three logic levels. These outputs transmitting gate and pull-up transistor are removed from the recommended inverter designs, which reduces the number of components. Transition times have improved and overall power consumption has been greatly lowered when ternary logic gates are implemented with a single source of power. Given the various advantages of the MVL, the optimum design of MVL gates is crucial for continued study and implementation in this area.

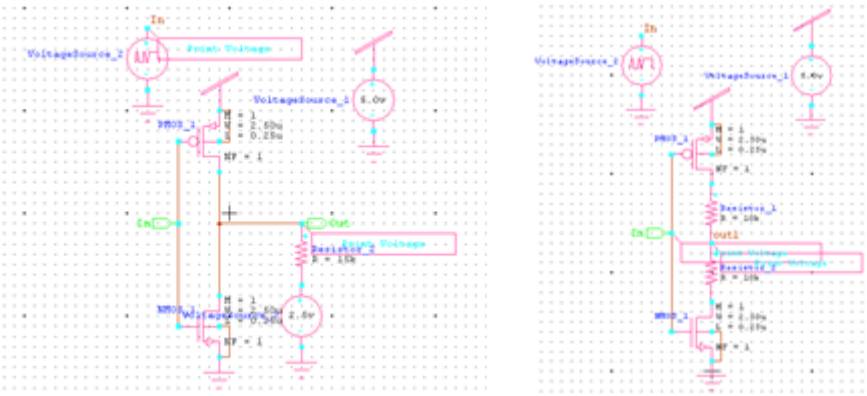

Figure1. Two types of TNOT schematic

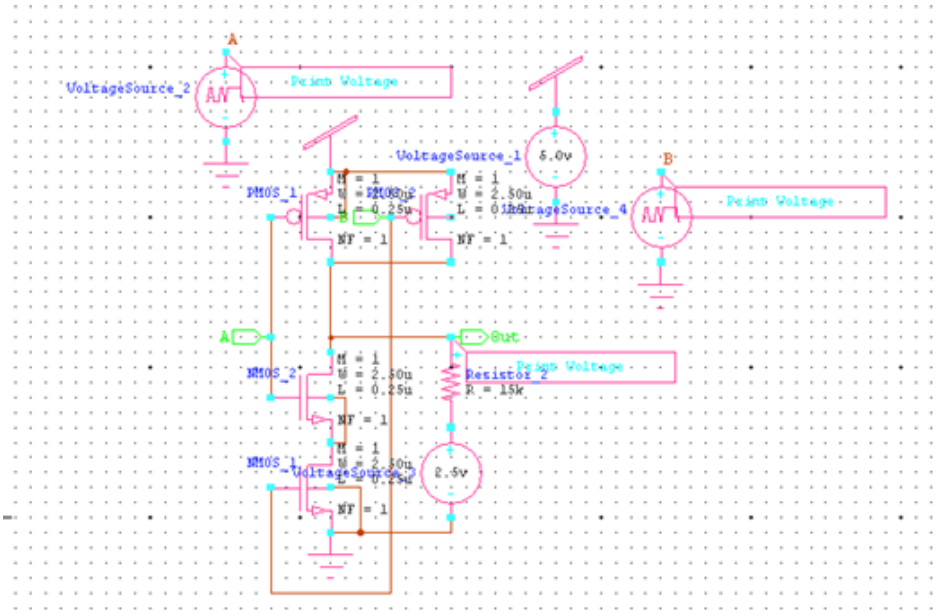

Figure2.Sample TNAND Schematic

i) *Ternary Adder*

The decoder's primary job is to select one of the three lines from our input when we give it instructions. Now that X and Y have been fed into two distinct Half-Adders, their outputs are fed into quaternary logic AND gate to produce various terms, which are then fed into the 2 input OR gate to produce the terms that make up the Sum-Of product (SOP). B is the ternary buffer gate's output in this example, and the final result of the ternary each multiplication is made up of two SOP inputs with Same gates—one from the binary buffer and one from the preceding OR gate.

$$Sum = X2Y0 + X1Y1 + X0Y2 + 1 \cdot (X1Y0 + X0Y1 + X2Y2) \quad (1)$$

$$Carry = 1 \cdot (X2Y1 + X2Y2 + X1Y2) \quad (2)$$

A ternary adder's primary task is to combine the two inputs (X and Y) and produce two results: sum and carry.

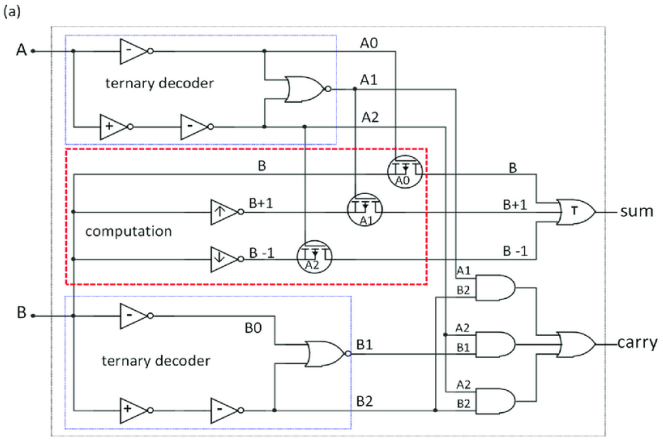

Figure3. Ternary Adder

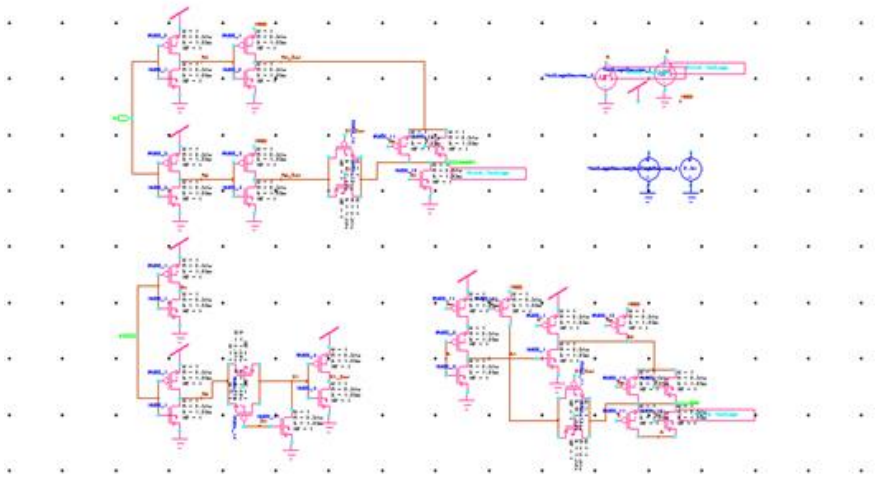

Figure4a. Proposed Ternary Single bit Adder Schematic

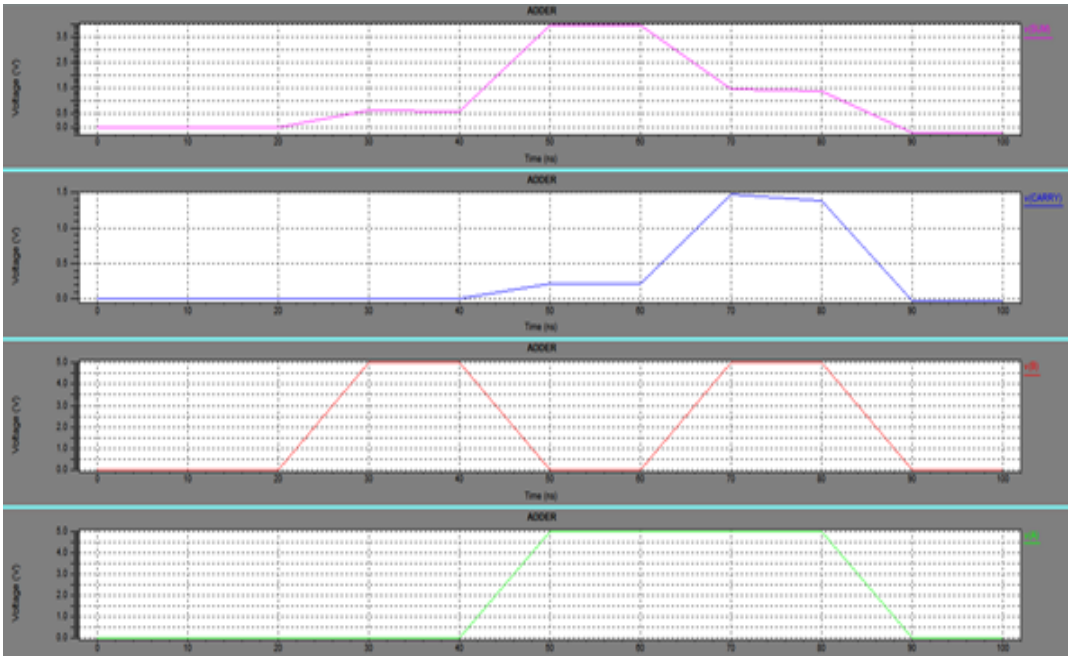

Figure4b. Proposed Ternary Single bit Adder Transient and Fourier analysis

i)Ternary Multiplier

The creation of partial products, shifting operations, and finally partial product addition are required for the multiplication of an n-bit ternary integer. A 1-bit ternary multiplier was combined with half and full Tadders to generate the multiplier block [9].

$$Mul = A_0^2B_0^1 + B_0^2A_0^1 + 1.(A_0^1B_0^1 + A_0^2B_0^2) \quad (3)$$

$$Carry = 1.(A_0^2 + B_0^2) \quad (4)$$

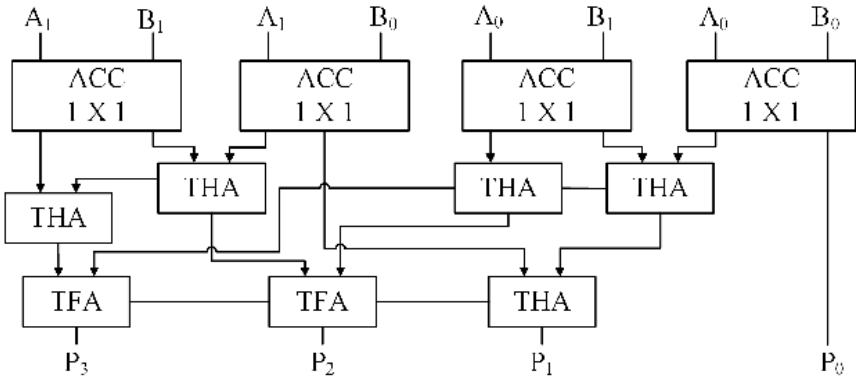

Figure5. Ternary Multiplier

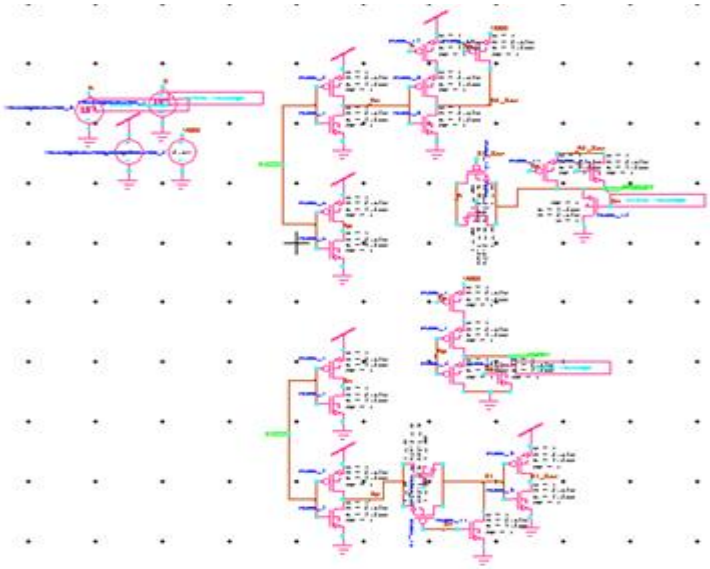

Figure6a. Proposed Ternary Single bit Multiplier Schematic

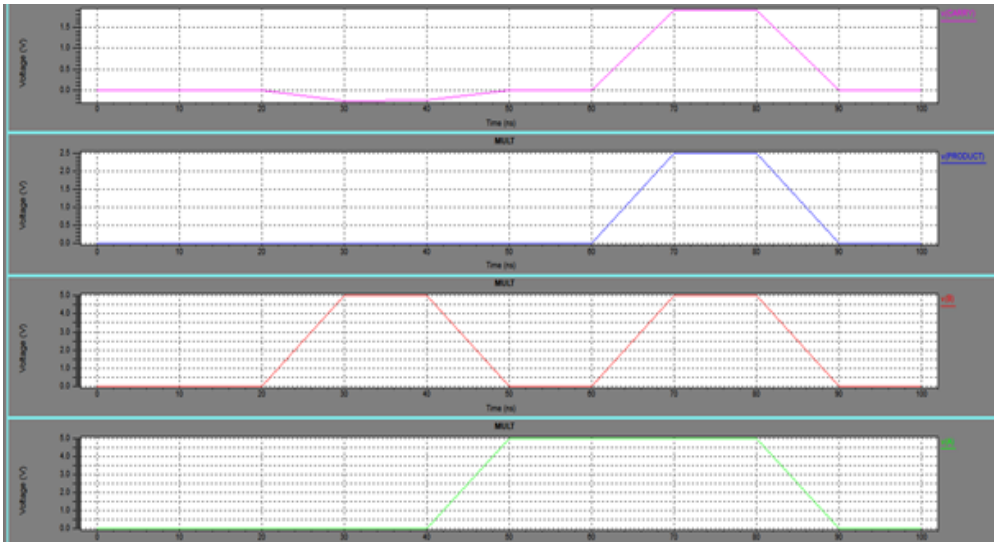

Figure6b. Proposed Ternary Single bit Multiplier Transient and Fourier analysis

ii) Result

According to reports, Tanner Tool could be used as EDA software to create and check VLSI circuits. The Tanner tool, version 13.02, is used to construct the Tgates created in this study on a PC with a core 2 duo processor running at 2 GHz and 1 GB of RAM. . The tanner tool's essential subgroups, S-Edit, L-Edit, T-Spice, and W-Edit, are used to create various device configurations and further assess the operation of the gates. The injected voltage method theoretically transforms the basic binary logic structure of the circuit's gates into equivalent ternary ones. Adopting these techniques to Biomedical sensor networks may reduce the device size and improves performance [14].

Table1. TERNARY GATES TIMING PARAMETERS.

Parameter	Level of logic	TADD	TMUL
Rise Period	0 to 1	2.31 ns	0.73 ns
Rise Period	1 to 2	1.46 ns	0.73 ns
Rise Period	0 to 2	0.49 us	1.68 us
Fall Season	2 to 0	2.49 us	0.49 us
Fall Season	2 to 1	2.09 ns	1.57 ns
Fall Season	1 to 0	0.72 ns	1.42 ns

Table2. THE TERNARY GATES' PERFORMANCE PARAMETERS

Average Strength	TADD	TMUL
TRANSISTOR MOS	1.217uw	0.288mw
Resistor	3.104uw	0.377 mw

	POWER	DELAY	PDP		POWER	DELAY	PDP
HFA	$4.956x10^{-4}$	$1.803x10^{-8}$	$8.935x10^{-12}$	**MUL**	$5.953x10^{-3}$	$9.760x10^{-8}$	$5.8101x10^{-10}$
THFA	$6.276x10^{-6}$	$1.080x10^{-8}$	$6.77x10^{-14}$	**TMUL**	$4.1261x10^{-6}$	$1.080x10^{-8}$	$4.456x10^{-14}$

IV. CONCLUSION

In this study, a ternary multiplier and ternary adder VLSI designs have been developed from an arithmetic perspective. Due to their pipelined design, the suggested ternary multiplication and ternary adder were able to operate at higher frequencies even with greater filter orders.NOR and NAND circuits are recognised as essential elements in the construction of electronic systems.By reducing power usage and propagation delay time, the number of transistors is primarily sought to be decreased. Implementing ternary logic gates with a single power source has reduced overall power dissipation significantly and improved transition times.The simulation results show that compared to previous ternary adders and multipliers, the recommended adder and multiplier uses fewer components and has a shorter delay.

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